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STRATEGIES IN OPTIMIZING MARKET POSITIONS FOR SEMICONDUCTOR VENDORS BASED ON IP LEVERAGE

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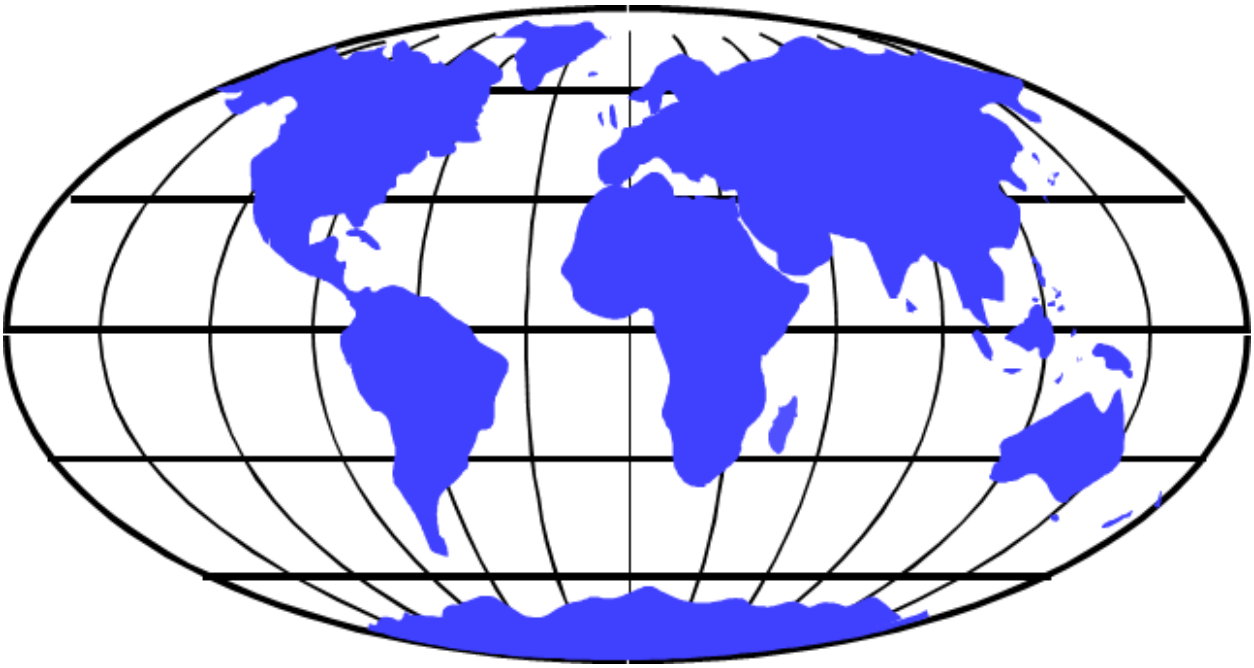

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1. Overview

The complexity of designs being implemented by semiconductor vendors continues to increase with the reduction in feature dimensions, with the ramp-up of 20nm and 16/14nn technologies. As designs become more complex, there is also a rise in the number and complexity of the embedded IP functionality, which can extend the time-to-market for new products unless the IP is thoroughly verified in silicon before being committed to designs.

The number and value of IP blocks within IC designs are increasing as the complexity of designs increases, which provide opportunities for companies that have access to key IP functionality to achieve high revenue growth.

As the number of IP blocks per design and the complexity of IP blocks increase, semiconductor companies are expected to increase outsourcing of IP access because of the superior financial returns from using their design engineers for implementing new designs rather than for developing industry standard IP blocks.

The embedded IP includes the following:

- ***Basic IP:*** Includes standard cells as well as building block functions. As feature dimensions are reduced to 28nm and 20nm, there is the need for close synergy between the characterization of basic IP blocks and the database of wafer manufacturing processes.

- ***Standards-based IP:*** Includes industry standards such as USB 3.0, 802.11ac, DDR4, and other functions. The complexity of standards-based IP is increasing rapidly as feature dimensions are reduced, with growing challenges in supporting IP development and qualification within the required time windows. The role of verification IP is increasing with the rise in complexity of standards-based IP, and as a result, it is beneficial for semiconductor vendors to utilize third-party IP vendors that have strong IP verification capabilities.

- ***Specialty IP:*** Includes both hardware functionality and algorithms such as LTE protocol stacks. Hardware IP, including processor engines such as ARM processors, Tensilica processors, ARC processors, Power Architecture, MIPS processors, and others, is also included in specialty IP. Specialty IP is often available from third-party companies, but there can be the need to harden the IP within the wafer processing environment where the products that have the embedded IP will be manufactured.

The above IP categories have different economic leverage factors for both semiconductor vendors and IP providers. An example is the higher up the IP is in the system value chain, the higher the value

leverage is that can be obtained by its IP vendors as well as by semiconductor vendors from integrating the IP in IC products.

A key strategic issue in the IP arena is the level of resources committed to developing IP by semiconductor vendors. If design engineering resources are limited, it can be better for semiconductor vendors to focus their efforts on developing new products rather than on IP development. It is from developing and selling products that semiconductor vendors generate revenues. Outsourcing the design and qualification of IP can provide better financial returns than developing and qualifying the IP internally.

If semiconductor vendors have access to unlimited design engineering resources, then both IP and products can be developed and verified. However, the reality is that semiconductor vendors only have access to limited design engineering resources, and with increased demand on engineering design resources, feature dimensions are reduced. There is, consequently, the need to establish priorities in committing engineering resources between IP development and product development, with the key metric being the financial return that can be obtained by semiconductor companies.

The Cadence specialty IP can provide competitive barriers that can give IC product price premiums, which can provide good financial returns for semiconductor vendors. ***There are benefits for semiconductor companies to make investments in having leadership capabilities in specialty IP. However, if the IP conforms to industry standard protocols where multiple IC companies have access to the IP, it can be a much better decision for IC vendors to outsource this IP and utilize design engineers to develop additional products.***

Another key factor that needs to be included in the IP development or licensing decision process is the time-to-market for the development of new products that can be slowed by the need to qualify the IP that is integrated in designs.

If there is the ability to obtain IP from third-party sources where the IP is already qualified by a mainstream foundry vendor, the time-to-market for new products can be much shorter than the IP that is developed and qualified internally by semiconductor vendors. By being early instead of late to the market, semiconductor vendors can obtain higher market share and higher prices for their products.

The decision to develop IP internally or to outsource the development and qualification of IP needs to be based on payback metrics at the semiconductor product and market share levels. Revenues are also obtained by semiconductor vendors from selling IC products. To gain price premiums from IC products, it is critical to optimize the positioning of IC products in the market.

2. IP Development and Verification Costs

A perspective on the cost of developing and verifying IP with the reduction in feature dimensions is shown in the following figures and tables.

FIGURE 1
Cost of Developing and Verifying IP with Reduction in Feature Dimensions (Leader)

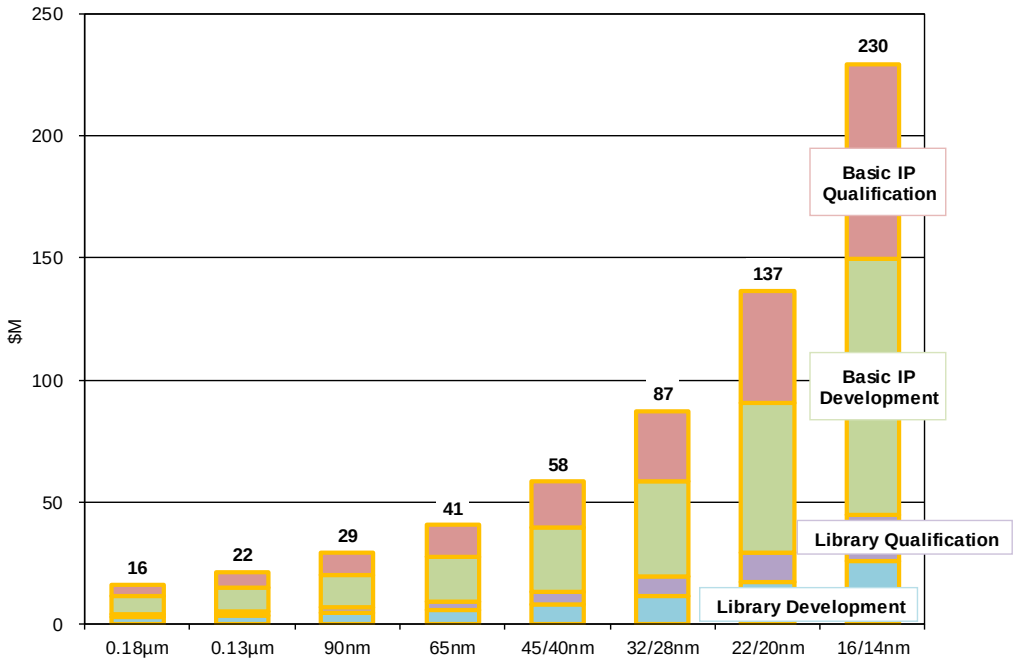


TABLE 1
Cost of Technology Participation with Reduction in Feature Dimensions (Leader)

	0.18µm	0.13µm	90nm	65nm	45/40nm	32/28nm	22/20nm	16/14nm
Library ($M)	**4.1**	**5.3**	**7.0**	**9.5**	**13.4**	**19.5**	**29.3**	**44.9**
• Growth rate (%)	NA	29.0	32.9	35.9	40.5	45.2	50.5	53.2
• Development ($M)	2.7	3.4	4.5	6.0	8.2	11.7	17.3	26.0
- Growth rate (%)	NA	27.6	30.7	33.4	37.8	42.6	47.5	50.5
• Qualification ($M)	1.4	1.9	2.6	3.6	5.2	7.8	12.0	18.9
- Growth rate (%)	NA	31.7	36.8	40.2	44.9	49.4	55.0	57.0
Basic IP ($M)	**12.3**	**16.3**	**22.2**	**31.0**	**45.0**	**68.0**	**107.2**	**184.6**
• Growth rate (%)	NA	32.4	36.5	39.6	45.1	50.9	57.7	72.2
• Development ($M)	7.4	9.7	13.1	18.1	26.1	39.1	61.5	104.7
- Growth rate (%)	NA	31.4	34.7	38.1	44.3	49.6	57.2	70.3
• Qualification ($M)	4.9	6.6	9.1	12.9	18.9	28.9	45.7	79.9
- Growth rate (%)	NA	33.8	39.1	41.7	46.2	52.8	58.4	74.7
TOTAL ($M)	**16.4**	**21.6**	**29.3**	**40.6**	**58.4**	**87.4**	**136.5**	**229.5**
• Growth rate (%)	NA	31.5	35.6	38.7	44.0	49.6	56.1	68.1

FIGURE 2
Cost of Participation with Reduction in Feature Dimensions (Follower)

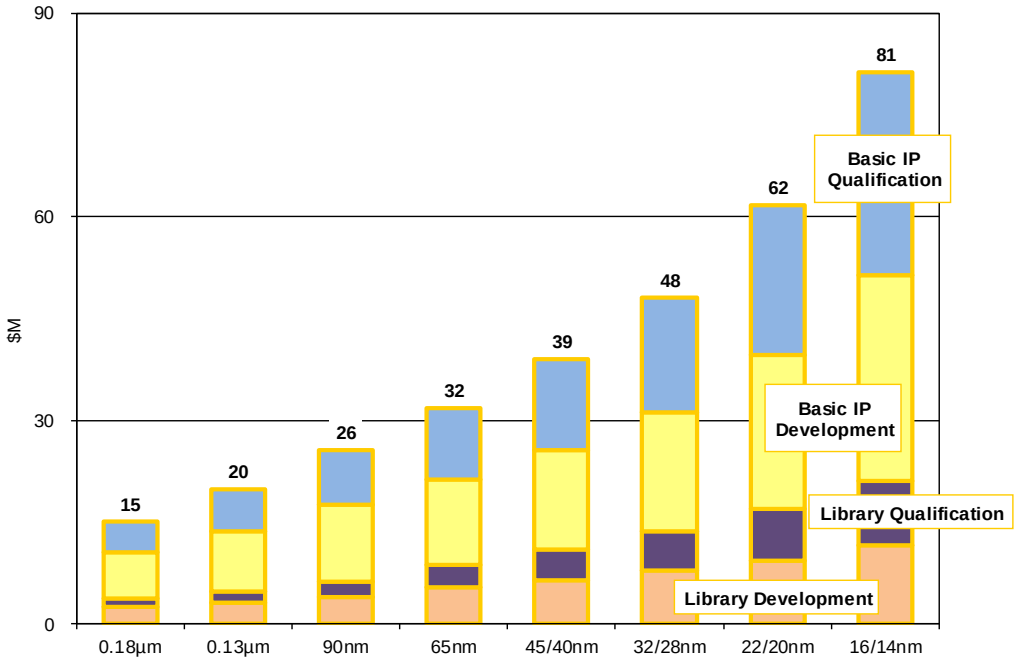


TABLE 2
Cost of Technology Participation with Reduction in Feature Dimensions (Follower)

	0.18µm	0.13µm	90nm	65nm	45/40nm	32/28nm	22/20nm	16/14nm
Library ($M)	**3.8**	**4.8**	**6.3**	**8.6**	**10.9**	**13.6**	**16.9**	**21.1**
• Growth rate (%)	NA	26.3	31.3	36.5	26.7	24.8	24.3	24.9
• Development ($M)	2.5	3.1	4.0	5.4	6.5	7.8	9.4	11.5
- Growth rate (%)	NA	24.0	29.0	35.0	20.4	20.0	20.5	22.3
• Qualification ($M)	1.3	1.7	2.3	3.2	4.4	5.8	7.5	9.6
- Growth rate (%)	NA	30.8	35.3	39.1	37.5	31.8	29.3	28.0
Basic IP ($M)	**11.3**	**15.1**	**19.4**	**23.3**	**28.2**	**34.4**	**44.8**	**60.2**
• Growth rate (%)	NA	33.6	28.5	20.1	21.0	22.0	30.2	34.4
• Development ($M)	6.8	8.9	11.2	12.7	14.7	17.6	22.7	30.2
- Growth rate (%)	NA	30.9	25.8	13.4	15.7	19.7	29.0	33.0
• Qualification ($M)	4.5	6.2	8.2	10.6	13.5	16.8	22.1	30.0
- Growth rate (%)	NA	37.8	32.3	29.3	27.4	24.4	31.5	35.7
TOTAL ($M)	**15.1**	**19.9**	**25.7**	**31.9**	**39.1**	**48.0**	**61.7**	**81.3**
• Growth rate (%)	NA	31.8	29.1	24.1	22.6	22.8	28.5	31.8

Key issues in the cost of IP development and qualification include the following:

- The cost of developing IP is shown for leaders and followers and includes the cost of libraries and basic IP, which are required for participation in different technology nodes. The cost of developing and qualifying application-specific or specialty IP is in addition to the levels shown.

  The analysis shows that the cost of developing libraries, which include standard cell building block functions, is increasing rapidly with the reduction in feature dimensions. To optimize performance and leakage, it is important to have close interfaces between the design environment and wafer processing environment. This means that the relationship with foundry vendors is critical for fabless semiconductor companies, but there are significant costs associated with building the manufacturing-aware expertise.

- Technology leaders are the companies that are early in adopting advanced feature technologies such as 20nm and 16/14nm and are forced to qualify most of the libraries and basic IP through close collaboration with foundry vendors. This can include collaboration on verifying the IP within wafer processes when they are ready for high volume production.

- Technology followers are companies that use new technologies 24 months after the leaders and are able to utilize the libraries and basic IP blocks that have been developed and qualified by foundry vendors. During this phase, the process is fully verified and is stable, with the initial design being in high volume production.

  Large cost savings are associated with being a follower, but there are challenges in achieving price premiums for their products in the market because competitors have already established their products. To displace incumbent vendors, there is the need to provide superior products or lower prices, and both can be difficult to achieve.

Strategies for IP development and qualification need to be closely aligned with the product strategies of IC vendors and with how IC vendors participate in the market.

The importance of IP continues to increase within the IC application solution environment as feature dimensions are reduced. This, in turn, requires the strategies that are used for IP qualification to provide competitive advantages with targeted end markets.

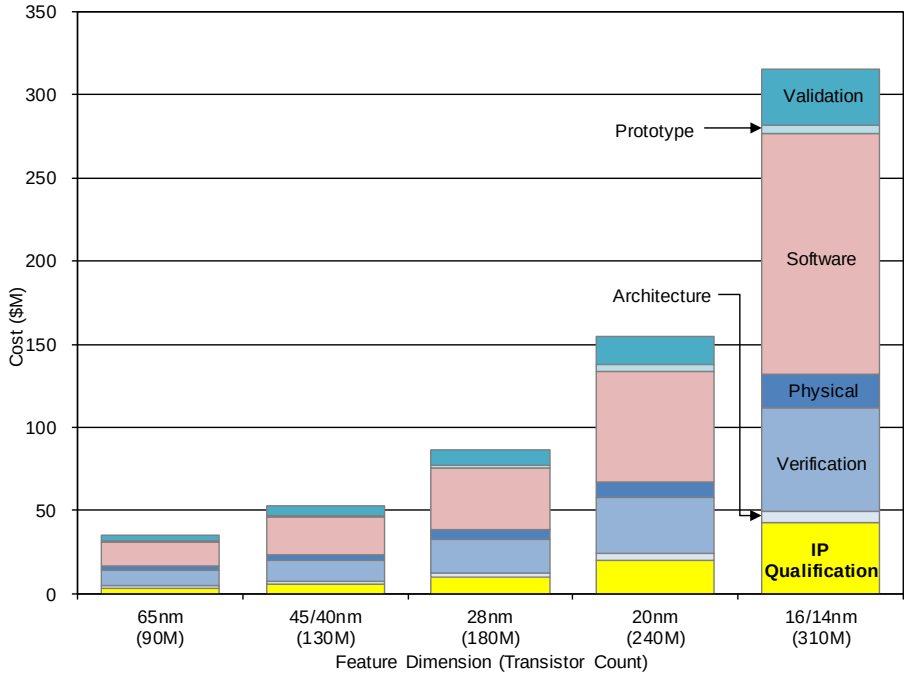
The increasing cost of developing and qualifying IP functionality in new technology nodes makes it increasingly attractive to collaborate with third-party IP vendors on building strong and competitive positions for semiconductor products within respective end markets. In comparison, using internal design engineering organizations to develop new products that generate additional revenues in the

market can provide better financial returns compared to using an engineer to develop the IP that is available from third-party vendors.

3. Strategic Issues within IC Design Environment

The cost of implementing IC designs is increasing with the reduction in feature dimensions, and a perspective on this increasing cost is shown in the following figure.

FIGURE 3
Design Cost Trends with Reduction in Feature Dimensions (Mainstream Designs)



Multiple cost categories are associated with implementing IC designs, but each category is experiencing higher costs as feature dimensions are reduced. The increase in design resources required with the reduction in feature dimensions can be supported by increasing the number of engineers that are allocated to new product designs or by lengthening the time-to-market for new products. However, there will likely be loss of market share and low profits from being late to the market within fast-moving markets.

In reality, all semiconductor companies are short of highly skilled design engineers, especially those that can implement complex designs in advanced technology nodes. Semiconductor vendors, consequently, can trade off the commitment of their engineering resources between designing new products (which provides revenues) or developing and qualifying IP (which in itself does not generate additional revenues from the market).

A key issue within many semiconductor companies is that IP development organizations have been established, and there is pressure to maintain these organizations because of the perceived strategic value in developing IP internally. However, it is important to determine how best to utilize the design engineering resources that are available to semiconductor vendors.

Strategic IP issues are, consequently, a combination of having access to the required IP portfolio and the integration of the IP within new IC products. Both capabilities are key parts of the IP environment and require access to financial and engineering resources. Key decisions, consequently, should be made on how to provide the best financial return at the product level.

4. Time-to-Market Strategic Factors

Many of the high growth segments of the semiconductor industry such as those in the mobile multimedia and consumer platforms have intense pressure on fast time-to-market for new products. However, there are large financial penalties for being late to the market with participation in fast-moving markets.

A perspective on the penalties of being late to market is shown in the following figure and table.

FIGURE 4
Penalties of Being Late to Market

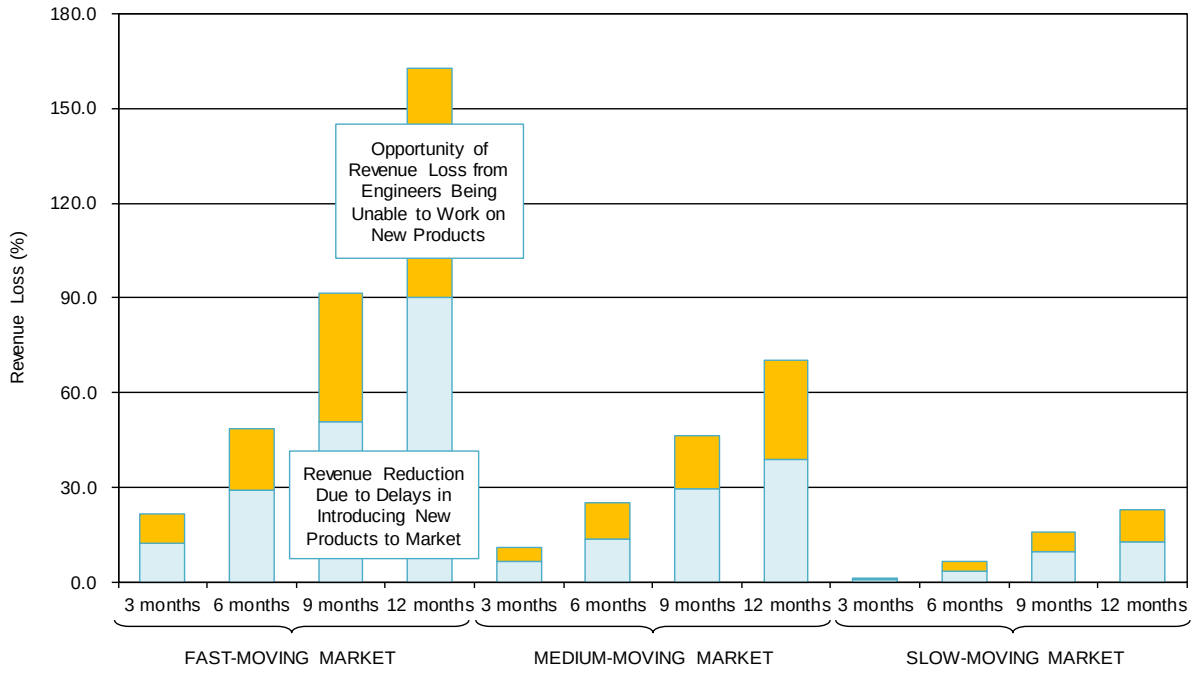


TABLE 3
Penalties of Being Late to Market

Market characteristics	3 months			6 months			9 months			12 months		
	Fast-moving market	Medium-moving market	Slow-moving market	Fast-moving market	Medium-moving market	Slow-moving market	Fast-moving market	Medium-moving market	Slow-moving market	Fast-moving market	Medium-moving market	Slow moving market
Revenue reduction due to delays in introducing new products to market	12.4	6.3	0.8	29.1	13.7	3.6	50.9	29.6	9.4	90.1	38.6	12.8
Opportunity of revenue loss from engineers being unable to work on new products	9.1	4.6	0.6	19.6	11.2	3.0	40.4	16.9	6.6	72.5	31.8	10.2
Revenue loss	21.5	10.9	1.4	48.7	24.9	6.6	91.3	46.5	16.0	162.6	70.4	23.0
Design engineering cost impact of delays in design completions	5.0	4.9	4.8	9.9	9.7	9.5	14.9	14.7	14.3	19.8	19.5	19.0

Semiconductor vendors' design methodologies, which include the development, qualification, and integration of IP, should be based on having fast time-to-market capabilities and on optimizing the position of new IC products in the market.

Key factors in the decision on whether to develop and qualify internal IP or to license IP from third-party companies should be based on the time-to-market of new products and the competitive positioning of new products within targeted applications.

If faster time-to-market for new products can be obtained from licensing IP compared to qualifying IP, it is clearly appropriate to license the IP.

High profits can be obtained from being an early market entry in fast-moving markets while low profits or losses can result from being late to the market. Having a strong market position has much higher value leverage compared to the cost of licensing third-party IP.

Financial decisions should determine the strategic decisions that are made regarding the positioning of companies within the IP environment, especially with the impact of the migration to feature dimensions such as 28nm, 20nm, and 16/14nm.

Similar perspectives also apply to specialty IP such as RF and analog-centric mixed-signal in mature process technologies such as 65nm, 130nm, and 180nm.

The decision to develop and qualify the IP versus licensing the IP should be based on market positioning, with different financial metrics for each technology node. However, it is expected that as feature dimensions are reduced, there will be increased value from licensing the IP from third-party companies.

5. Memory IP

The slowdown in enhancements in the performance of memory cores with the reduction in feature dimensions is placing increased emphasis on memory interfaces, which include various versions of DDR3, DDR4, and DDR5. There are also increased activities in Hybrid Memory Cube (HMC) and Wide I/O2, which represent technologies that will be used within some high throughput applications in the future.

The key requirement is to enhance system throughput while reducing power consumption, and with the reduction in feature dimensions, memory interfaces and controller architectures are becoming increasingly important in optimizing system performances.

NAND Flash interfaces are also being enhanced to support the high performance requirements of enterprise applications.

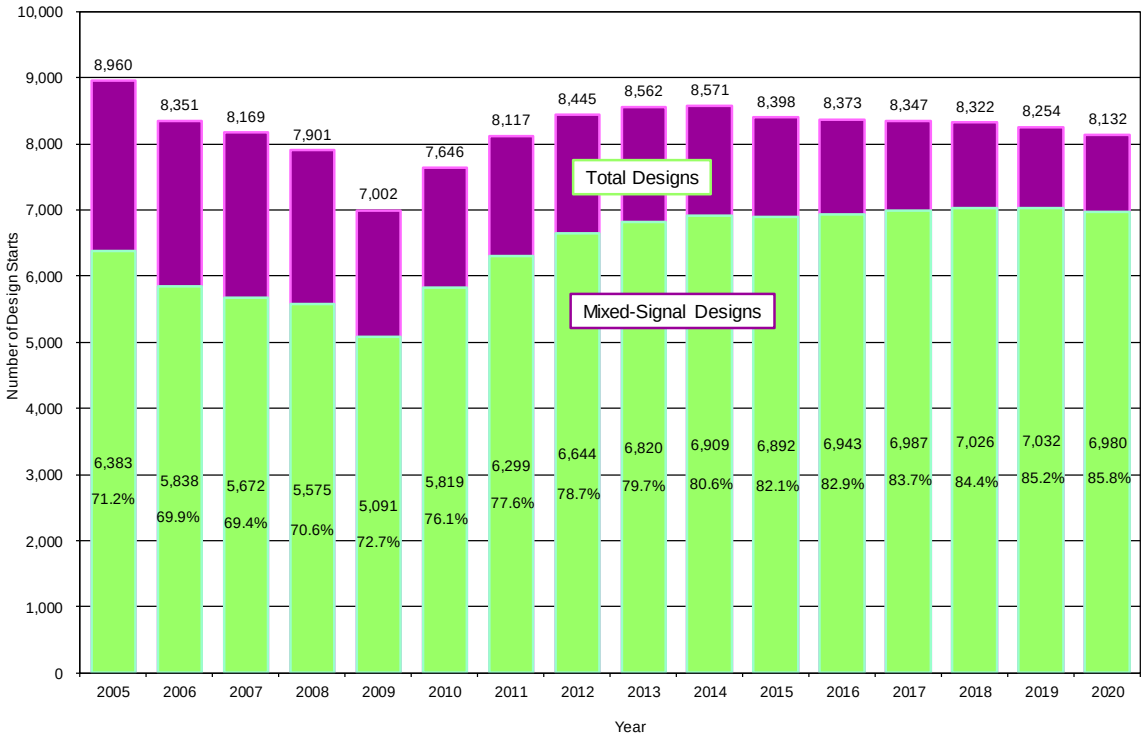
The pressure to enhance memory throughput has the need for changes in system architectures as well as for higher performance interfaces.

Cadence's capabilities in memory hierarchy IP are leadership on a global basis, which can support the bridge between processors and memory blocks as well as provide the ability to enhance system throughput and minimize power consumption.

6. Mixed-Signal IP Strategic Issues

Mixed-signal IP has a wide range of characteristics, with an increase in strategic importance as the complexity of IC products increases. A perspective on the number of IC design starts and the percentage of mixed-signal design starts is shown in the following figure.

FIGURE 5
Number of Mixed-signal Design Starts



The large number of mixed-signal design starts is driven by the need to interface with digital processing engines and analog characteristics of the real world environment. Also, a large number of interface functionalities need to be supported within the multimedia environment. The development and qualification of mixed-signal IP are engineering intensive and can require a pass in silicon to fully verify the characteristics of IP.

The result is that there are financial benefits for semiconductor vendors to collaborate with IP vendors that can supply qualified IP and for semiconductor vendors to use their high value engineers to develop products that can generate revenues from the market.

The decision to develop versus license IP is not only based on the incremental cost of developing and qualifying mixed-signal IP but also on the market position and market share that can be generated from being early to the market with new products.

7. Financial Metrics Summary

The analysis of the financial metrics that relate to semiconductor vendors is shown in the following table.

TABLE 4
Comparison of Financial Metrics

	A leader	B follower	C leader	D follower
Revenues ($), nominal level	100	100	100	100
Product development cost as percent of revenues (%)	10	10	20	20
Gross profit as percent of revenues (%) • Leader	50		50	
• Follower		30		30
SG&A as percent of revenues (%) • Leader	10		10	
• Follower		12		12
Operating income as percent of revenues (%)	30	8	20	(2)
IP cost as percent of selling price (%) • External	10		10	
• Internal		3		3
Net financial impact	+20*	5	+10**	(5)

Note:
* Very strong financial performance.
** Acceptable financial performance.

Four case studies are shown to demonstrate the financial metrics associated with the combination of leader and follower as well as the impact of the internal development of IP or licensing IP.

The quantitative analysis shows that gross profit margin can be 50% if the semiconductor company is early to the market compared to 30% if the semiconductor company is late to the market with new products.

As shown by the case study, if the cost of licensing IP is 10% of revenues compared to the financial impact of 3% of revenues for internal IP development, the financial benefit of being early to the market and having a strong market position is much better than the higher incremental cost of licensing IP.

Being late to the market can cause SG&A to be higher than an early-to-market company because of the need to displace competitors, which can require high selling costs.

The payback analysis is done for constant revenues, but the reality is that revenues will be higher if there is the ability to be early to the market, which provides greater financial benefits than the levels shown.

IP strategies have a major impact on the financial performance of semiconductor vendors. It is clear that unless major competitive advantages are obtained from having internal IP such as FPGA IP, there are large financial benefits in collaborating with third-party IP vendors in order to develop the design methodologies that can support fast time-to-market for new products.

8. Summary

IP strategies can have a major impact on the financial performance of semiconductor vendors, with increased effect as feature dimensions are reduced.

Semiconductor companies that make large investments in developing and qualifying IP instead of optimizing the position of their products in the market can experience negative financial returns from this decision. While having control over unique IP that establishes defensible competitive barriers has high value, most IP is available from third-party companies, and key issues are requirements in efficient integration of IP in new products and having fast time-to-market design disciplines.

In addition to having access to the appropriate IP, there is the need to have highly efficient approaches to integrating and verifying IP within IC products in order to reduce time-to-market for new products. New semiconductor products also need to have a very high probability of first-time success in targeted systems, which means that there is the requirement for access to verification IP that is thoroughly proven.

Cadence has gained access to a broad base of IP that is strategically important for many designs. The key IP in Cadence include memory interfaces, digital signal processors, and mixed-signal functionality.

Cadence is the ideal partner for semiconductor companies that want to optimize market positions in market segments that are IP intensive, where fast time-to-market for new designs is important. In addition to IP blocks and verification IP, there is the need to have highly efficient approaches to integrate the IP within IC designs, with a high probability of first-time success for designs.

The use of Cadence verification and emulation technologies and tools can provide strong competitive advantages to the semiconductor vendors that are astute in optimizing the use of these capabilities for their complex designs.

Biography

Dr. Handel Jones is the founder and CEO of International Business Strategies, Inc. (IBS), which is based in Los Gatos (California) and has been in business for over 25 years. IBS is active in quantifying the cost of implementing and manufacturing IC designs and financial metrics related to market positioning. IBS provides support to many global leaders in key areas of technologies, markets, and business strategies for the semiconductor and electronics industries.

Dr. Jones is also the author of *Chinamerica*, which was published by McGraw-Hill and provides insight into the drivers for the economy of the U.S. and China.